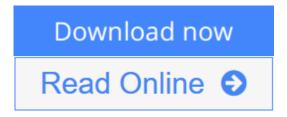


Adaptive Analog VLSI Neural Systems

By M. Jabri, R.J. Coggins, B.G. Flower



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amplitude ~---. -----. -----, -----, VfT:j." 4. 50 4. 00 3. 50 q . 3. 00 //. ~-"":!.2.50;:...1!-.i""""2.001.50.GO.O_O_,-...&.,.;DQ.".../ 1. 00 0. 50 0. 00 L. ----1. . --- . 1. ----:::""::-::-::-::-'-:::-::-:--=-::-'-::-= =""=_:' 5. 00 10. 00 15. 00 Figure 7. 1 The morphology of ST and VT retrograde 1:1. © 1995 IEEE [Coggins, labri, Flower and Pickard {1995}]. ing to the analog domain. Additionally, the use of differential pair multipliers and current node summing in the network allows a min imum of devices in the network itself and hence associated savings in power and area. However, in the last few decades analog signal processing has been used sparingly due to the effects of device off sets, noise and drift*. The neural network architecture alleviates these problems to a large extent due to the fact that it is both highly parallel and adaptive. The fact that the network is trained to recognize morphologies with the analog circuits in-loop means that the synaptic weights can be adapted to cancel device offsets [Castro, Tam and Holler (1993); Castro and Sweet (1993)]. The impact of local un correlated noise is reduced by the parallelism of * Most fabrication processes have been optimised for digital design techniques which results in poor analog performance.



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