



## Verilog Designer's Library (Prentice Hall Modern Semiconductor Design Series)

By Bob Zeidman

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Ready-to-use building blocks for integrated circuit design.

Why start coding from scratch when you can work from this library of pre-tested routines, created by an HDL expert? There are plenty of introductory texts to describe the basics of Verilog, but *Verilog Designer's Library* is the only book that offers real, reusable routines that you can put to work right away.

*Verilog Designer's Library* organizes Verilog routines according to functionality, making it easy to locate the material you need. Each function is described by a behavioral model to use for simulation, followed by the RTL code you'll use to synthesize the gate-level implementation. Extensive test code is included for each function, to assist you with your own verification efforts.

Coverage includes:

- Essential Verilog coding techniques
- Basic building blocks of successful routines
- State machines and memories
- Practical debugging guidelines

Although *Verilog Designer's Library* assumes a basic familiarity with Verilog structure and syntax, it does not require a background in programming. Beginners can work through the book in sequence to develop their skills, while experienced Verilog users can go directly to the routines they need. Hardware designers, systems analysts, VARs, OEMs, software developers, and system integrators will find it an ideal sourcebook on all aspects of Verilog development.

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## **Editorial Review**

From the Inside Flap

Preface

Hardware Description Languages (HDLs) are fast becoming the design method of choice for electrical engineers. Their ability to model and simulate all levels of design, from abstract algorithms and behavioral functions to register transfer level (RTL) and gate level descriptions, make them extremely powerful tools. Synthesis software allows engineers to take these very high-level descriptions of chips and systems and automatically convert them to real netlists for manufacturing, at least in theory. As chip complexity increases, and gate counts commonly reach 100,000 and above, HDLs become the only practical design method. Even FPGA densities have increased to the point where HDLs are the most efficient design entry method. The benefits of HDLs are even trickling into the areas of PCB design, where it is useful to have one set of tools for simulating integrated circuits and PCBs and the systems into which they are incorporated. The value of using HDLs to model a system on a behavioral level also cannot be ignored as system architects use them to determine and eliminate bottlenecks and improve overall performance of a wide variety of systems. WHAT IS THIS BOOK ABOUT?

Of the HDLs available, Verilog is one of the most popular. Many designs have been created in Verilog and a large number of Verilog simulators, compilers, synthesizers, and other tools are available from numerous vendors. Its powerful features have led to many applications in all areas of chip design.

This book provides a library of general purpose routines that simplify the task of Verilog programming and enhance existing designs. I have taken input from other designer engineers to make sure that this library covers many of the common functions that a hardware designer is likely to need. Beginning Verilog designers can use these routines as tutorials in order to learn the language or to increase their understanding of it. Experienced Verilog designers can use these routines as a reference and a starting point for real world designs. Rather than redevelop code for common functions, you can simply cut and paste these routines and modify them for your own particular needs. Each routine includes a brief but complete description plus fully documented Verilog code for Behavioral and Register Transfer Level (RTL) implementations. In addition, the Verilog simulation code that was used to verify each hardware module is also included. This code is also available on the enclosed diskette. Feel free to include the Verilog code, royalty-free, in your own designs. HOW IS THIS BOOK ORGANIZED?

The routines are organized according to functionality. Each chapter addresses a common type of function such as state machines, memory models, or data flow. Each section of a chapter gives an example of code to implement that particular function. Also, successive sections, in general, have increasingly more complex examples. Each function is described using a behavioral model followed by an RTL model. Because behavioral models do not include low level implementation details, they simulate very fast and can be used for quickly evaluating a proposed architecture for a chip or a system. The behavioral models are also useful for creating a simulation environment for your design. The inputs to a chip can be stimulated using behavioral models that might represent something simple, like DRAMs connected to a microprocessor, or something complex like workstations connected to a network. The RTL code, on the other hand, is needed to create real hardware. It is written with synthesis in mind. Despite the sophistication of many synthesis tools, these programs need to make decisions about the gate level implementation based on the RTL code. For this reason, the RTL descriptions must be written in such a way so that there is no ambiguity with respect to what

the designer has in mind. Also, the Verilog simulation code is given that is used to test the functionality of each module. This is important because good simulation code will determine whether the hardware will work correctly.

The organization of the book has another advantage. If you are a novice Verilog designer, you can start by studying the simple examples in the beginning and work your way up to the complex examples toward the end. This will give you a very comprehensive understanding of Verilog. If you are an experienced Verilog designer, you can simply jump right to the section that most closely matches your particular design needs. Take that function, play with it, and modify it to suit your design. This will save a significant amount of time by eliminating the need to write the code from scratch.

WHO IS THIS BOOK FOR?

This book is for Verilog users at any level. It assumes a basic familiarity with Verilog structure and syntax. It does not assume any programming background. The book is particularly well suited to hardware designers learning Verilog without having written programs previously, as well as those who have used languages such as BASIC, C, FORTRAN, or Pascal. The book will also appeal to experienced Verilog designers who can skip to the sections that fit their own needs.

This book is valuable to hardware designers, systems analysts, students, teachers, trainers, vendors, system integrators, VARs, OEMs, software developers, and consultants. It is an ideal follow-on or sourcebook for those who have just completed an introductory book or course on Verilog programming.

SUPPORT,  
SOURCE DISKS, AND COMMENTS

I have simulated all of the examples using SILOS III version 99.115 from Simucad Inc. All of the RTL code has been synthesized using FPGA Express version 3.4 from Synopsys, Inc. As with all published programs, there will surely be last minute changes, which appear on the README.TXT file on the accompanying diskette.

The publisher and I welcome your comments regarding the routines in the book. If you find bugs, discover better ways to accomplish tasks, or can suggest other routines that you think should be included, I am eager to hear about them. To receive notification of revisions and upgrades to the Library, please mail the registration form that appears later in this book.

Bob Zeidman  
Cupertino, California

From the Back Cover

Ready-to-use building blocks for integrated circuit design. Why start coding from scratch when you can work from this library of pre-tested routines, created by an HDL expert? There are plenty of introductory texts to describe the basics of Verilog, but "Verilog Designer's Library" is the only book that offers real, reusable routines that you can put to work right away. "Verilog Designer's Library" organizes Verilog routines according to functionality, making it easy to locate the material you need. Each function is described by a behavioral model to use for simulation, followed by the RTL code you'll use to synthesize the gate-level implementation. Extensive test code is included for each function, to assist you with your own verification efforts. Coverage includes:

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systems analysts, VARs, OEMs, software developers, and system integrators will find it an ideal sourcebook on all aspects of Verilog development.

#### About the Author

**Bob Zeidman** is the founder, president and CEO of The Chalkboard Network ([www.chalknet.com](http://www.chalknet.com)), a company that provides training for high-tech professionals via the Internet. Previously, Bob was the president of Zeidman Consulting where he designed ASICs, FPGAs, and PC boards for various real-time systems. His clients included Apple Computer, Cisco Systems, Ricoh Systems, and Texas Instruments. He has written technical papers on hardware and software design methods, and has taught courses on Verilog, ASIC design, and FPGA design at conferences throughout the world. He holds a Master's degree from Stanford University and two Bachelor's degrees from Cornell University.

#### Users Review

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##### **Samantha Campbell:**

Here thing why this specific Verilog Designer's Library (Prentice Hall Modern Semiconductor Design Series) are different and reliable to be yours. First of all studying a book is good but it depends in the content of the usb ports which is the content is as yummy as food or not. Verilog Designer's Library (Prentice Hall Modern Semiconductor Design Series) giving you information deeper since different ways, you can find any guide out there but there is no reserve that similar with Verilog Designer's Library (Prentice Hall Modern Semiconductor Design Series). It gives you thrill reading journey, its open up your own eyes about the thing that will happened in the world which is maybe can be happened around you. It is possible to bring everywhere like in park your car, café, or even in your method home by train. When you are having difficulties in bringing the printed book maybe the form of Verilog Designer's Library (Prentice Hall Modern Semiconductor Design Series) in e-book can be your substitute.

##### **Benjamin Martinez:**

This Verilog Designer's Library (Prentice Hall Modern Semiconductor Design Series) is brand-new way for you who has interest to look for some information given it relief your hunger info. Getting deeper you upon it getting knowledge more you know or perhaps you who still having little digest in reading this Verilog Designer's Library (Prentice Hall Modern Semiconductor Design Series) can be the light food for you personally because the information inside this kind of book is easy to get by simply anyone. These books create itself in the form and that is reachable by anyone, that's why I mean in the e-book form. People who think that in e-book form make them feel drowsy even dizzy this book is the answer. So there is absolutely no in reading a e-book especially this one. You can find what you are looking for. It should be here for an individual. So , don't miss this! Just read this e-book sort for your better life along with knowledge.

##### **Melissa Sands:**

That reserve can make you to feel relax. This particular book Verilog Designer's Library (Prentice Hall Modern Semiconductor Design Series) was multi-colored and of course has pictures around. As we know that book Verilog Designer's Library (Prentice Hall Modern Semiconductor Design Series) has many kinds

or category. Start from kids until teens. For example Naruto or Private eye Conan you can read and think that you are the character on there. So , not at all of book usually are make you bored, any it offers up you feel happy, fun and unwind. Try to choose the best book for you personally and try to like reading this.

### **Ricky Bradley:**

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