



# The gm/ID Methodology, a sizing tool for low-voltage analog CMOS Circuits: The semi-empirical and compact model approaches (Analog Circuits and Signal Processing)

By Paul Jespers

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IC designers appraise currently MOS transistor geometries and currents to compromise objectives like gain-bandwidth, slew-rate, dynamic range, noise, non-linear distortion, etc. Making optimal choices is a difficult task. How to minimize for instance the power consumption of an operational amplifier without too much penalty regarding area while keeping the gain-bandwidth unaffected in the same time? Moderate inversion yields high gains, but the concomitant area increase adds parasitics that restrict bandwidth. Which methodology to use in order to come across the best compromise(s)? Is synthesis a mixture of design experience combined with cut and tries or is it a constrained multivariate optimization problem, or a mixture? Optimization algorithms are attractive from a system perspective of course, but what about low-voltage low-power circuits, requiring a more physical approach? The connections amid transistor physics and circuits are intricate and their interactions not always easy to describe in terms of existing software packages.

The gm/ID synthesis methodology is adapted to CMOS analog circuits for the transconductance over drain current ratio combines most of the ingredients needed in order to determine transistors sizes and DC currents.

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## **Editorial Review**

From the Back Cover

How to determine transistor sizes and currents when the supply voltages of analog CMOS circuits do not exceed 1.2V and transistors operate in weak, moderate or strong inversion? The  $g_m/I_D$  methodology offers a solution provided a reference transconductance over drain current ratio is available. The reference may be the result of measurements carried out on real physical transistors or advanced models. The reference may also take advantage of a compact model. In *The  $g_m/I_D$  Methodology, a Sizing Tool for Low-Voltage Analog CMOS Circuits*, we compare the semi-empirical to the compact model approach. Small numbers of parameters make the compact model attractive for the model paves the way towards analytic expressions unaffordable otherwise. The E.K.V model is a good candidate, but when it comes to short channel devices, compact models are either inaccurate or loose straightforwardness. Because sizing requires basically a reliable large signal representation of MOS transistors, we investigate the potential of the E.K.V model when its parameters are supposed to be bias dependent. The model-driven and semi-empirical methods are compared considering the Intrinsic Gain Stage and a few more complex circuits. A series of MATLAB files found on [extras-springer.com](http://extras-springer.com) allow redoing the tests.

About the Author

Dr. Paul Jespers is Professor Emeritus at UCL, Louvain-la-Neuf, Belgium, and has been visiting professor at Stanford ('67-'69) and UC Berkeley ('90-'91).

He has co-authored several books, and in 2001 published "Integrated Digital-to-Analog and Analog-to-Digital Converters" which was published by Wiley (ISBN 0-19-856446-5)

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